SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

(Approved by AICTE, New Delhi& Affiliated to JNTUA, Ananthapuramu)

(Accredited by NBA for Civil, EEE, Mech., ECE & CSE)

(Accredited by NAAC with 'A+' Grade)

Puttur -517583, Tirupati District, A.P. (India)

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

Master of Technology in VLSI

SEMESTER - I

S.No.	Course Code	Subject	Category	L	T	P	Credits
1	25EC4201	CMOS Analog IC Design	PC	3	0	0	3
2	25EC4202	CMOS Digital IC Design	PC	3	0	0	3
Program Elective – I							
3	25EC4203	Microchip Fabrication Techniques	PE	3	0	0	3
	25EC4204	Scripting Languages for VLSI	PE				
	25EC4205	CAD for VLSI	PE				
Program Elective – II							
4	25EC4206	Device Modelling	PE	3	0	0	3
5	25EC4207	FPGA Architectures and Applications	PE				
6	25EC4208	ASIC Design	PE				
7	25EC4209	CMOS Analog IC Design Lab	PC	0	0	4	2
8	25EC4210	CMOS Digital IC Design Lab	PC	0	0	4	2
9	25ME3111	Research Methodology and IPR	MC	2	0	0	2
10	25EC4211	RTL Synthesis, Simulation and Verification	SE	0	1	2	2
Audit Course – I							
11	25EC4232	English for Research Paper Writing	AC	2	0	0	0
	25CE1031	Disaster Management	AC				
	25CS5831	Essence of Indian Traditional Knowledge	AC				
Total				**16**	**1**	**10**	**20**

SEMESTER - II

S.No.	Course Code	Subject	Category	L	T	P	Credits
1	25EC4212	CMOS Mixed Signal IC Design	PC	3	0	0	3
2	25EC4213	Physical Design Automation	PC	3	0	0	3
Program Elective – III							
3	25EC4214	SoC Testing and Verification	PE	3	0	0	3
	25EC4215	Semiconductor Memory Design and Testing	PE				
	25EC4216	Advanced VLSI interconnects	PE				
Program Elective – IV							
4	25EC4217	Low Power VLSI Design	PE	3	0	0	3
5	25EC4218	Algorithms for VLSI Design	PE				
6	25EC4219	VLSI Signal Processing	PE				
7	25EC4220	CMOS Mixed Signal IC Design Lab	PC	0	0	4	2
8	25EC4221	Physical Design Automation Lab	PC	0	0	4	2
Mandatory Course							
9	25CS5822	Quantum Technologies and Applications	MC	2	0	0	2
10	25EC4222	Comprehensive Viva Voce	PC	0	1	2	2
Audit Course – II							
11	25EE2130	Pedagogy Studies	AC	2	0	0	0
	25EE2131	Personality Development Through Life Enlightenment Skills	AC				
	25CS5832	Yoga For Stress Management	AC				
Total				**16**	**1**	**10**	**20**

SEMESTER - III

S.No.	Course Code	Subject	Category	L	T	P	Credits
Program Elective – V							
3	25EC4223	Bi-CMOS Technology and Applications	PE	3	0	0	3
	25EC4224	Optimization Techniques and Applications in VLSI Design	PE				
	25EC4225	SoC Architecture	PE				
4	25EC4226	**Open Elective – I** IoT and its applications	OE	3	0	0	3
7	25EC4227	Dissertation Phase – I	PR	0	0	20	10
8	25EC4228	Industry Internship		0	0	0	2
9	20EC4229	Co-curricular Activities		0	0	0	1
		Total		**06**	**0**	**20**	**19**

SEMESTER – IV

S.No.	Course Code	Subject	Category	L	T	P	Credits
1.	25EC4230	Dissertation Phase – II	PR	0	0	32	16
		Total		**0**	**0**	**32**	**16**

NOTE: L-Lecture, T- Tutorial, P-Practical

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(25EC4201) CMOS ANALOG IC DESIGN

COURSE OBJECTIVES:

The objectives of this course

1. *This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.*
2. *Basic design concepts, issues and tradeoffs involved in analog IC design are explored.*
3. *Intuitive understanding and real-life applications are emphasized throughout the course.*
4. *To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.*
5. *To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Design MOSFET based analog integrated circuits.*
2. *Analyze analog circuits at least to the first order.*
3. *Appreciate the trade-offs involved in analog integrated circuit design.*
4. *Understand and appreciate the importance of noise and distortion in analog circuits.*
5. *Analyze complex engineering problems critically in the domain of analog IC design for conducting research.*
6. *Solve engineering problems for feasible and optimal solutions in the core area*

UNIT-I

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT-II

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair wit MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit.

UNIT-III

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT-IV

DSA Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT-V

Operational Amplifiers: One Stage Op-Amp, Two Stage Op-Amp, Gain Boosting, Common Mode Feed-Back, Input Range Limitations, Slew Rate, PSRR. Compensation of Two Stage Op-Amp, Slewing in Two Stage Op-Amp, Compensation Techniques. Design Procedure for 2-Stage Op-Amp.

TEXT BOOKS:

1. *B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition 2016.*
2. *Paul.R.Gray & Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5thEdition, 2009.*

REFERENCES:

1. *B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition 2016.*
2. *Paul.R.Gray & Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5thEdition, 2009.*

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(25EC4202) CMOS DIGITAL IC DESIGN

COURSE OBJECTIVES:

The objectives of this course

1. *To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.*
2. *The course also involves analysis of performance metrics.*
3. *To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.*
4. *To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,*
2. *Estimate Delay and Power of Adders circuits.*
3. *Classify different semiconductor memories.*
4. *Analyze, design and implement combinational and sequential MOS logic circuits.*
5. *Analyze complex engineering problems critically in the domain of digital IC design for conducting research.*
6. *Solve engineering problems for feasible and optimal solutions in the core area of digital ICs*

UNIT-I

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT-IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. *Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010*
2. *Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.*
3. *CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.*

REFERENCES:

1. *Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011*
2. *Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2ndEdition, PHI.*

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(25EC4203) MICROCHIP FABRICATION TECHNIQUES
Program Elective – I

COURSE OBJECTIVES:

The objectives of this course

1. *Comprehend impact of semiconductor industry on the design of development of integrated circuits.*
2. *Acquaint with clean room technology*
3. *Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.*
4. *Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and*
5. *45nm technologies*
6. *Understand packaging principles*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Understand various stages of fabrication*
2. *Understand various packaging techniques and Design rules.*
3. *Classify various thin films and its characteristics.*

UNIT-I

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT-II

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT-III

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT-IV

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT-V

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.

Packaging: Chip characteristics, package functions, package operations.

TEXTBOOKS:

1. *Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.*
2. *Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.*

REFERENCES:

1.C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

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(25EC4204) SCRIPTING LANGUAGES FOR VLSI
Program Elective – I

COURSE OBJECTIVES:

The objectives of this course

1. *Learn programming with scripting languages*
2. *Understand how to create and run scripts using PERL/TCL/PYTHON in CAD Tools*
3. *Gain knowledge about PERL/PYTHON/ TCL in developing system and web applications*
4. *Develop skill to design a real time project using PERL/PYTHON*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Gain fluency in programming with scripting languages*
2. *Create and run scripts using PERL/TCL/PYTHON in CAD Tools*
3. *Demonstrate the use of PERL/PYTHON/ TCL in developing system and web applications*
4. *Develop a real time project using PERL/PYTHON*

UNIT-I

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages**..**

UNIT-II

PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-III

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues.

UNIT-IV

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT-V

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.

PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.

TEXT BOOKS:

1.The World of Scripting Languages- David Barron, Wiley Student Edition.
2.PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications.

REFERENCES:

1. TCL/TK: A Developer's Guide- ClifFlynt, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition.

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(25EC4205) CAD FOR VLSI
Program Elective – I

COURSE OBJECTIVES:

The objectives of this course

1. *To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.*
2. *To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.*
3. *To practice the application of fundamentals of VLSI technologies*
4. *To optimize the implemented design for area, timing and power by applying suitable constraints.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1 *Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.*
2 *Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.*
3 *Practice the application of fundamentals of VLSI technologies*
4 *Optimize the implemented design for area, timing and power by applying suitable constraints.*

UNIT-I

Introduction: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II

Partitioning: Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT-III

Floor Planning: Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV

Placement and Routing: Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of

routing algorithms, Single layer routing algorithms.

UNIT-V

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

TEXT BOOKS:

1. *Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.*
2. *CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.*

REFERENCES:

1. *VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.*
2. *Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.*
3. *VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition*

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(25EC4206) DEVICE MODELLING
Program Elective – II

COURSE OBJECTIVES:

The objectives of this course

1. *To understand the physics of 2-terminal MOS operation and its characteristics*
2. *To understand the physics of 4-terminal MOSFET operation and its characteristics.*
3. *To analyze the SOI MOSFET electrical characteristics.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1 *Understand the physics of 2-terminal MOS operation and its characteristics*
2 *Understand the physics of 4-terminal MOSFET operation and its characteristics.*
3 *Analyze the SOI MOSFET electrical characteristics.*

UNIT-I

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of of, Φms and Dit.).

UNIT-II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT-III

4-terminal MOSFET: Threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT-IV

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT-V

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

TEXT BOOKS:

1. *S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.*

2. *M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.*

REFERENCES:

1. *Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.*
2. *E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.*
3. *J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009*

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(25EC4207) FPGA ARCHITECTURES AND APPLICATIONS
Program Elective – II

COURSE OBJECTIVES:

The objectives of this course

1. *To acquire knowledge about various architectures and device technologies of PLD's.*
2. *To comprehend FPGA Architectures.*
3. *To analyze System level Design and their application for Combinational and Sequential Circuits.*
4. *To familiarize with Anti-Fuse Programmed FPGAs.*
5. *To apply knowledge of this subject for various design applications.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1 *Acquire knowledge about various architectures and device technologies of PLD's.*
2 *Comprehend FPGA Architectures.*
3 *Analyze System level Design and their application for Combinational and Sequential Circuits.*
4 *Familiarize with Anti-Fuse Programmed FPGAs.*
5 *Apply knowledge of this subject for various design applications.*

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT-IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT-V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

TEXT BOOKS:

1. *Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.*
2. *Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.*

REFERENCES:

1. *Field Programmable Gate Arrays-John V. Oldfield, Richard C. Dorf, Wiley India.*
2. *Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.*
3. *Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes.*
4. *FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.*

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(25EC4208) ASIC DESIGN

Program Elective – II

COURSE OBJECTIVES:

The objectives of this course

1. *To understand different types of ASICs and their libraries.*
2. *To understand about programmable ASICs, I/O modules and their interconnects.*
3. *To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Understand different types of ASICs and their libraries.*
2. *Understand about programmable ASICs, I/O modules and their interconnects.*
3. *Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.*

UNIT – I

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT – II

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT – III

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT – IV

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT – V

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

TEXT BOOKS:

1. *Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.*
2. *L.J. Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.*

REFERENCES:

1. *Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001.*

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(25EC4209) CMOS ANALOG IC DESIGN LAB

COURSE OBJECTIVES:

The objectives of this course is to

1. *To explain the VLSI Design Methodologies using VLSI design tool.*
2. *To grasp the significance of various CMOS analog circuits in full-custom IC Design flow*
3. *To explain the Physical Verification in Layout Design*
4. *To fully appreciate the design and analyze of analog and mixed signal simulation*
5. *To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation*

COURSE OUTCOMES (COs):

Upon successful completion of this course, students will be able to:

1. *Explain the VLSI Design Methodologies using VLSI design tool.*
2. *Grasp the significance of various CMOS analog circuits in full-custom IC Design flow*
3. *Explain the Physical Verification in Layout Design*
4. *Fully appreciate the design and analyze of analog and mixed signal simulation*
5. *Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation*

List of Experiments:

The students are required to design and implement using CMOS Technology.
The students are required to implement LAYOUTS of any SIX Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Two stage Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

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(25EC4210) CMOS DIGITAL IC DESIGN LAB

COURSE OBJECTIVES

The objectives of this course is to

1. *To explain the VLSI Design Methodologies using any VLSI design tool.*
2. *To grasp the significance of various design logic Circuits in full-custom IC Design.*
3. *To explain the Physical Verification in Layout Extraction.*
4. *To fully appreciate the design and analyze of CMOS Digital Circuits.*
5. *To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.*

COURSE OUTCOMES (COs)

Upon successful completion of this course, students will be able to:

1. *Explain the VLSI Design Methodologies using any VLSI design tool.*
2. *Grasp the significance of various design logic Circuits in full-custom IC Design.*
3. *Explain the Physical Verification in Layout Extraction.*
4. *Fully appreciate the design and analyze of CMOS Digital Circuits.*
5. *Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.*

List of Experiments:

The students are required to design and implement the Circuit and Layout of any Twelve Experiments using CMOS Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

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(25ME3111) RESEARCH METHODOLOGY AND IPR

COURSE OBJECTIVES:

The objectives of this course

1. *To understand the research design process and data collection methods.*
2. *To develop skills in data analysis and reporting.*
3. *To familiarize students with intellectual property rights (IPR) and patents.*
4. *To apply research skills in real-world contexts.*
5. *Understand the intricacies of grant of patent, patentability, licensing and revocation at national and international level.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Recall key concepts and terminology related to research design, data collection, and intellectual property rights.*
2. *Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.*
3. *Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.*
4. *Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.*
5. *Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods.*
6. *Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property*

UNIT – I

FUNDAMENTALS OF RESEARCH METHODOLOGY: Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

UNIT – II

DATA COLLECTION AND SOURCES: Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

UNIT – III

DATA ANALYSIS AND REPORTING: Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

UNIT – IV

UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS: Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT – V

PATENTS: Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

TEXT BOOKS:

1. *Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004*
2. *2.Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007*

REFERENCES:

1. *Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).*
2. *Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.*
3. *Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.*
4. *Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024*
5. *The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.*
6. *Peter Elbow, Writing With Power, Oxford University Press, 1998.*

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(25EC4211) RTL SYNTHESIS, SIMULATION AND VERIFICATION

COURSE OBJECTIVES

The objectives of this course is to

1. *The simulation of combinational and sequential circuits.*
2. *FSM based designs.*
3. *Implementation of DFT and FFTs.*
4. *Verify layout of basic digital circuits.*

COURSE OUTCOMES (COs)

On successful completion of this course, students will be able to

1. *Demonstrate the process steps required for simulation /synthesis.*
2. *Design and simulate various combinational and sequential circuits using HDL.*
3. *Develop an RTL code for various real time applications.*
4. *Synthesize / Simulate an RTL code for several digital designs*
5. *Build and verify various digital circuits.*

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (SystemVerilog/VHDL basics).
- Lab:

1. Write synthesizable Verilog/SystemVerilog code for:

a) Half Adder, Full Adder
b) 4-bit Ripple Carry Adder
c) 4-bit Synchronous Counter (Up/Down)

2. FSM Design: Sequence Detector (e.g., detect “1011”).

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:

1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
2. Generate gate-level netlist and analyze area, delay, power reports.
3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Testbench creation, waveforms, debugging.
- Lab: Run simulations

1. Develop testbenches for:

a) 4-bit ALU (add, sub, AND, OR).
b) Universal Shift Register.

2. Perform functional simulation using EDA tools
3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification testbenches.

1. Write self-checking testbenches for combinational and sequential circuits.
2. Use assertion-based verification (SystemVerilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a digital subsystem such as:

1. UART Transmitter/Receiver
2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
3. FIFO Buffer with full/empty flags

Textbooks / References

1. *Samir Palnitkar – Verilog HDL: A Guide to Digital Design and Synthesis.*
2. *Michael Ciletti – Advanced Digital Design with the Verilog HDL.*
3. *Chris Spear & Greg Tumbush – SystemVerilog for Verification.*
4. *David Rich – Design and Verification with SystemVerilog.*

Suggested reading:

1. *Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall 2003.*
2. *Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.*
3. *Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books, 2002.*

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(25EC4232) ENGLISH FOR RESEARCH PAPER WRITING

(Audit Course-I)

COURSE OBJECTIVES:

The objectives of this course

1. *To equip students with the fundamentals of academic English for research paper writing.*
2. *To develop students' advanced reading skills for analyzing and evaluating research articles.*
3. *To refine students' grammar and language skills for clarity and precision in research writing.*
4. *To master the skills of revising, editing, and proofreading research papers.*
5. *To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Recall the key language aspects and structural elements of academic writing in research papers.*
2. *Explain the importance of clarity, precision, and objectivity in research writing.*
3. *Apply critical reading strategies and advanced grammar skills to analyze and write research papers.*
4. *Analyze research articles and identify the strengths and limitations of different methodologies.*
5. *Evaluate research papers to check for plagiarism, structure, clarity, and language accuracy.*
6. *Evaluate the effectiveness of different language and technology tools in research writing, including AI-assisted tools and plagiarism detection software.*
7. *Develop a well-structured research paper that effectively communicates complex ideas.*

UNIT – I

Fundamentals of Academic English: Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT – II

Reading Skills for Researchers: Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT – III

Grammar Refinement for Research Writing: Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT – IV

Mastery in Refining Written Content/Editing Skills: Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

UNIT – V

Technology and Language for Research: Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

TEXT BOOKS:

1. *1.Bailey. S. Academic Writing: A Handbook for International Students. London and*
2. *New York: Routledge,2015.*
3. *Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.*

REFERENCES:

1. *Craswell, G. Writing for Academic Success, Sage Publications, 2004.*
2. *Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007*
3. *Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005*
4. *Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills*
5. *and Tasks. Michigan University Press, 2012.*
6. *5.Goldbort R.Writing for Science, Yale University Press (available on Google Books), 2006*
7. *Day R.How to Write and Publish a Scientific Paper, Cambridge University Press, 2006*

ONLINE LEARNING RESOURCES:

1. *https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/*
2. *https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview*
3. *"Writing in the Sciences" – Stanford University (MOOC on Coursera) https://www.coursera.org/learn/sciwrite*
4. *Academic Phrasebank – University of Manchester http://www.phrasebank.manchester.ac.uk*
5. *OWL (Online Writing Lab) – Purdue University, https://owl.purdue.edu *(Resources on APA/MLA formats, grammar, structure, paraphrasing)**
6. *Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources.*

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(25CE1031) DISASTER MANAGEMENT

(Audit Course-I)

COURSE OBJECTIVES:

The objectives of this course

1. *To enable the students to understand the fundamental concepts of disasters, hazards, their factors, and significance with special reference to India.*
2. *To prepare them to classify and analyze different types of natural and man-made disasters, their causes, magnitude, and impacts.*
3. *To foster them develop understanding of disaster preparedness, monitoring systems, and the role of government, community, and media.*
4. *To equip them in learning risk assessment techniques, disaster risk reduction strategies, and the importance of global and national cooperation.*
5. *To foster their ability to think critically and respond to disasters and design effective mitigation measures (structural and non-structural) with a focus on emerging trends and Indian disaster management programs.*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Define and distinguish between hazards and disasters, and explain their types, nature, and impacts.*
2. *Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters.*
3. *CAssess the economic, social, and ecological repercussions of major natural and man-made disasters.*
4. *Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness.*
5. *Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels.*
6. *Formulate and evaluate structural and non-structural disaster mitigation strategies, with emphasis on Indian programs and emerging trends.*

UNIT – I

Introduction: Disaster - Definition, Factors and Significance - Difference Between Hazard and Disaster - Natural and Man-made Disasters - Difference, Nature, Types and Magnitude - Disaster Prone Areas in India - Study of Seismic Zones - Areas Prone to Floods and Droughts, Landslides and Avalanches - Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami - Post-Disaster Diseases and Epidemics.

UNIT – II

Repercussions of Disasters and Hazards Economic Damage - Loss of Human and Animal Life - Destruction of Ecosystem - Natural Disasters - Earthquakes, Volcanism, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster - Nuclear Reactor Meltdown - Industrial Accidents - Oil Slick sand Spills - Outbreaks of Disease and Epidemics War and Conflicts

UNIT – III

Disaster Preparedness and Management: Preparedness - Monitoring of Phenomena - Triggering a Disasteror Hazard - Evaluation of Risk-Application of Remote Sensing - Data from Meteorological and Other Agencies - Media Reports- Governmental and Community Preparedness

UNIT – IV

Risk Assessment: Disaster Risk -Concept and Elements, Disaster Risk Reduction - Global and National Disaster Risk Situation -Techniques of Risk Assessment – Global Co-Operation in Risk Assessment and Warning - People's participation in Risk Assessment – Strategies for Survival

UNIT – V

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation - EmergingTrends in Mitigation - Structural Mitigation and Non- Structural Mitigation - Programs of Disaster Mitigation in India

TEXT BOOKS:

1. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.
2. Gupta, H. K. Disaster Management. Universities Press, 2003

REFERENCES:

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.
4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.
5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

ONLINE LEARNING RESOURCES:

1. National Disaster Management Authority (NDMA), India: https://ndma.gov.in – official guidelines, reports, and policy frameworks.
2. United Nations Office for Disaster Risk Reduction (UNDRR): https://www.undrr.org – Sendai Framework, global risk reduction strategies.
3. Global Disaster Alert and Coordination System (GDACS): https://www.gdacs.org – real-time disaster alerts.

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(25CS5831) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE

(Audit Course-I)

COURSE OBJECTIVES:

The objectives of this course

1. *To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.*
2. *To make them understand the need for protecting traditional knowledge and its significance in the global economy.*
3. *To make them understand the legal frame work and policies related to traditional knowledge protection.*
4. *To enable them to understand the relationship between traditional knowledge and intellectual property rights.*
5. *To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology*

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. *Define and explain the concept of traditional knowledge, its nature, characteristics, and scope*
2. *Understand the need for protecting traditional knowledge and its significance in the global economy*
3. *Explain the legal framework and policies related to traditional knowledge protection*
4. *Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology*
5. *Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change*
6. *Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms*

UNIT – I

Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge -Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

Learning Outcomes:

UNIT – II

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

UNIT – III

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

UNIT – IV

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT – V

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

TEXT BOOKS:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. *Introduction to Indian Knowledge System: Concepts and Applications*, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh,*Traditional Knowledge System and Technology in India,* PratibhaPrakashan 2012.

REFERENCES:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. *Indian Astronomy: A Source Book*, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. *History of Technology in India*, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. *Indian Architecture*, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. *Public Administration in Ancient India*, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,*Indian Knowledge Systems Vol – I & II,* Indian Institute of Advanced Study, Shimla, H.P., 2022

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(25EC4212) CMOS MIXED SIGNAL IC DESIGN

COURSE OBJECTIVES:

The objectives of this course

1. To demonstrate first order filter with least interference
2. To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
3. To design different A/D, D/A, modulators, demodulators and different filter for real time applications.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Demonstrate first order filter with least interference
2. Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
3. Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT – I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators.

UNIT – II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT – III

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT – IV

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D converters, Time- interleaved converters.

UNIT – V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

Textbooks:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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(25EC4213) PHYSICAL DESIGN AUTOMATION

COURSE OBJECTIVES:

The objectives of this course

1. To understand relation between automation algorithms and constraints posed by VLSI technology.
2. To adopt algorithms to meet critical design parameters.
3. To design area efficient logics by employing different routing algorithms and shape functions.
4. To simulate and synthesis different combinational and sequential logics.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand relation between automation algorithms and constraints posed by VLSI technology.
2. Adopt algorithms to meet critical design parameters.
3. Design area efficient logics by employing different routing algorithms and shape functions.
4. Simulate and synthesis different combinational and sequential logics.

UNIT – I

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT – II

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT – III

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT – IV

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT – V

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

Reference Books:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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(25EC4214) SoC TESTING AND VERIFICATION
(Program Elective – III)

COURSE OBJECTIVES:

The objectives of this course

1. To understand the concepts of faults and testing in SoC
2. To implement the faults using simulation tools
3. To analyze BIST systems

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand the concepts of faults and testing in SoC
2. Implement the faults using simulation tools
3. Analyze BIST systems

UNIT – I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT – II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT – III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT – IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT – V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. M.L. Bushnell, V. D. Agrawal, —Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits‖, Kluwer Academic Publishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, —Digital Systems and Testable Design‖, Jaico Publishing House.

Reference Books:

1. P.K. Lala, —Digital Circuits Testing and Testability‖, Academic Press.

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(25EC4215) SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Program Elective – III)

COURSE OBJECTIVES:

The objectives of this course

1. To understand different types of memories, their architectural and different packing techniques of memories.
2. To build fault models for memory testing.
3. To analyze different parameters that lead malfunctioning of memories.
4. To design reliable memories with efficient architecture to improve processes times and power.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
2. Build fault models for memory testing.
3. Analyze different parameters that lead malfunctioning of memories.
4. Design reliable memories with efficient architecture to improve processes times and power.

UNIT – I

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT – II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, Onetime programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT – III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT – IV

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and

Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT – V

Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Textbooks:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.

Reference Books:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, First Edition. Prentice hall.

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(25EC4216) ADVANCED VLSI INTERCONNECTS
(Program Elective – III)

COURSE OBJECTIVES:

The objectives of this course

1. Gain insight into transmission line parameters of VLSI interconnects.
2. Understand novel and emerging solutions for future VLSI interconnect technologies.
3. Learn the impact of inductive effects in high-speed interconnects.
4. Know the effect of quantum effects in nano scale interconnects.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand the transmission line parameters of VLSI interconnect.
2. Learn the novel and emerging solutions for future VLSI interconnect technologies.
3. Analyze the impact of inductive effects in high-speed interconnects.
4. Examine the influence of quantum effects in nano scale interconnects.

UNIT – I

Introduction: Introduction to VLSI Interconnects, The Distributed RC Interconnect Model, Elmore Delay in Interconnects, Scaling Effects in Interconnects, Simulation and Delay Mitigation in RC Interconnects.

UNIT – II

Inductive Effects: Inductive Effects in Interconnects, Distributed RLC Interconnect Model, Transmission Line Equations, When to Consider the Inductive Effects, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, RLC Interconnect Simulation.

UNIT – III

Resistance at High Frequencies, Power Dissipation due to Interconnects, Electromigration in Interconnects, Mitigation of Electromigration.

UNIT – IV

Crosstalk: Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, Mitigation Techniques, Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance, Extraction of Inductance, Estimation of Interconnect Parameters from S-parameters.

UNIT – V

Quantum Effects: Quantum Conductance, Quantum Capacitance, Kinetic Inductance, Graphene Nanoribbon Interconnects, Analysis and Simulation of Interconnect Considering Quantum Effects.

Textbooks:

1. Ashok K. Goel, High-Speed VLSI Interconnects.
2. Y.S.Diamand, Advanced Nanoscale ULSI Interconnects: Fundamental sand Applications,

Reference Books:

1. H.S Philip Wong and DejiAkinwande, Carbon nanotube and Graphene Device Physics, 2011.

Other Suggested Readings:
NPTEL Courses (https://onlinecourses.nptel.ac.in/noc22_ee125/preview)

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(25EC4217) LOW POWER VLSI DESIGN
(Program Elective – IV)

COURSE OBJECTIVES:

The objectives of this course

1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. To implement Low power design approaches for system level and circuit level measures.
3. To design low power adders, multipliers and memories for efficient design of systems.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. Implement Low power design approaches for system level and circuit level measures.
3. Design low power adders, multipliers and memories for efficient design of systems.

UNIT – I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT – IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf

Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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(25EC4218) ALGORITHMS FOR VLSI DESIGN
(Program Elective – IV)

COURSE OBJECTIVES:
The objectives of this course
1. To understand the VLSI design methodologies
2. To understand the optimization methods
3. To learn various methodologies in floor planning
4. To explore the tools used in Physical Design Automation

COURSE OUTCOMES (COs):
On successful completion of this course, students will be able to
1. Understand the VLSI design methodologies
2. Understand the optimization methods
3. Learn various methodologies in floor planning
4. Explore the tools used in Physical Design Automation

UNIT – I
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT – II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT – III
LAYOUT COMPACTION, PLACEMENT, FLOOR PLANNING AND ROUTING
Problems, Concepts and Algorithms.
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT – IV
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High level Transformations.

UNIT – V
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full

Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

Textbooks:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.1999.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., Springer International Edition, 2005.

Reference Books:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill &Peterson, Wiley, 1993.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd Ed., Pearson Education Asia, 1998.

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(25EC4219) VLSI SIGNAL PROCESSING
(Program Elective – IV)

COURSE OBJECTIVES:

The objectives of this course

1. To study the existing architectures suitable for VLSI.
2. To understand the concepts of folding and unfolding algorithms and applications.
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Study the existing architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Design new architectures suitable for VLSI.
4. Implement fast convolution algorithms.

UNIT – I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT – II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multi rate systems Unfolding-Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT – III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT – IV

Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT – V

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

Textbooks:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998.

2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, Prentice Hall, 1985.

Reference Books:

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing, Prentice Hall, 1994.
2. Medisetti V. K, VLSI Digital Signal Processing, IEEE Press (NY), 1995.

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(25EC4220) CMOS MIXED SIGNAL IC DESIGN LAB

COURSE OBJECTIVES:

The objectives of this course

1. To design and simulate op-amp for given specifications
2. To design and simulate data converter for given specifications
3. To design and simulate PLL and VCO for given specifications
4. To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Design and simulate op-amp for given specifications
2. Design and simulate data converter for given specifications
3. Design and simulate PLL and VCO for given specifications
4. Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of the following Experiments using CMOS Technology.

Cycle 1:

1. Fully compensated op-amp with resistor and miller compensation
2. High speed comparator design
    a) Two stage cross coupled clamped comparator
    b) Strobed Flip-flop
3. Data converter

Cycle 2:

1. Switched capacitor circuits
    a) Parasitic sensitive integrator
    b) Parasitic insensitive integrator
2. Design of PLL
3. Design of VCO
4. Band gap reference circuit
5. Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS Op Amp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

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(25EC4221) PHYSICAL DESIGN AUTOMATION LAB

COURSE OBJECTIVES:

The objectives of this course

1. To learn the implementation of different Physical Design Automation algorithms
2. To implement different graph algorithms
3. To implement different partitioning algorithms
4. To implement different floor planning algorithms
5. To implement different routing algorithms

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Learn the implementation of different Physical Design Automation algorithms
2. Implement different graph algorithms
3. Implement different partitioning algorithms
4. Implement different floor planning algorithms
5. Implement different routing algorithms

List of Experiments:

Cycle 1:

1. Graph algorithms
    a) Graph search algorithms
        i. Depth first search
        ii. Breadth first search
    b) Spanning tree algorithm
        i. Kruskal's algorithm
    c) Shortest path algorithm
        i. Dijkstra algorithm
        ii. Floyd- Warshall algorithm
    d) Steiner tree algorithm
2. Computational geometry algorithm
    a) Line sweep method
    b) Extended line sweep method

Cycle 2:

3. Partitioning algorithms
    a) Group migration algorithms
        I. Kernighan –Lin algorithm
        II. Extensions of Kernighan-Lin algorithm
            i. Fiduccias –Mattheyses algorithm
            ii. Goldberg and Burstein algorithm
    b) Simulated annealing and evolution algorithms
        i. Simulated annealing algorithm
        ii. Simulated evolution algorithm
        iii. Metric allocation method
4. Floor planning algorithms
    i. Constraint based methods
    ii. Integer programming based methods
    iii. Rectangular dualization based methods

iv. Hierarchical tree based methods
v. Simulated evolution algorithms
vi. Time driven Floor planning algorithms

5. Routing algorithms
   I. Two terminal algorithms
      a) Maze routing algorithms
         i. Lee's algorithm
         ii. Soukup's algorithm
         iii. Hadlock algorithm
      b) Line-Probe algorithm
      c) Shortest path based algorithm
   II. Multi terminal algorithm
      a) Stenier tree based algorithm
         i. SMST algorithm
         ii. Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Text Books:

1. Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

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(25CS5822) QUANTUM TECHNOLOGIES AND APPLICATIONS
(Mandatory Course)

COURSE OBJECTIVES:

The objectives of this course

1. Present core quantum principles such as superposition and entanglement without mathematical formalism.
2. Develop conceptual clarity on qubits, quantum states, and information frameworks.
3. Examine the theoretical challenges in realizing scalable quantum systems.
4. Introduce foundational ideas in quantum communication and computing.
5. Highlight applications, industrial adoption, and future research directions in quantum technologies.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Upon completion, the learner will be able to:
2. Explain fundamental quantum concepts conceptually.
3. Distinguish classical information systems from quantum information frameworks. Identify the principal theoretical limitations in building quantum computers.
4. Describe the conceptual basis of quantum communication and computation.
5. Discuss current applications, technological trajectories, and career opportunities in the quantum domain.

Unit-I: Foundations of Quantum Theory and Technologies

Transition from classical to quantum physics. Key conceptual principles: Superposition, Entanglement, Uncertainty, Wave-particle duality. Quantum states and measurement; the role of the observer. Representative quantum systems: electrons, photons, atoms. Concept of quantization and discrete energy levels. Strategic relevance of quantum technologies.

Overview of major domains: Computing, Communication, Sensing. Global quantum initiatives: India's National Quantum Mission, EU Quantum Flagship, USA, China.

Unit-II: Conceptual Structure of Quantum Information

Qubits: qualitative understanding using spin and polarization. Classical bits vs quantum bits: distinctions and implications. Quantum systems (non-engineering perspective): trapped ions, superconducting qubits, photonics. Coherence and decoherence mechanisms. Abstract notions: quantum states, measurement operators, Hilbert space—interpretation without mathematics. Entanglement and non-locality as foundational resources. Quantum vs classical information principles; philosophical considerations.

Unit-III: Building a Quantum Computer – Challenges and Requirements

Conceptual prerequisites for functional quantum hardware. Fragility of quantum states: decoherence, noise, stability issues. Requirements: isolation, error resilience, scalability, control. Why maintaining entanglement is difficult; theoretical necessity of quantum error correction. Comparative overview of hardware platforms (superconducting circuits, trapped ions, photonics).Current progress vs scientific constraints; conceptual view of quantum software's role.

Unit-IV: Quantum Communication and Computing

(Redundant explanations removed, retaining only unique themes.)Quantum vs classical communication paradigms. Essentials of Quantum Key Distribution (QKD) and its security rationale. Entanglement-enabled communication protocols. Concept of the Quantum Internet and secure global networking. Introduction to quantum computing and quantum parallelism.

Conceptual comparison of classical and quantum gate operations. Challenges: decoherence, noise, and the necessity of error correction frameworks.

Unit-V: Applications, Industry, and Future Directions

Application domains: Healthcare and drug discovery, Material science and chemistry, Optimization and logistics, Quantum sensing and precision timing. Case studies: IBM, Google, Microsoft, PsiQuantum. Ethical, societal, and policy considerations. Barriers to adoption: cost, skilled workforce, standards. Emerging research and career landscapes; India's strategic opportunity in the global quantum ecosystem.

Textbooks

1. Nielsen & Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010.
2. Rieffel & Polak, Quantum Computing: A Gentle Introduction, MIT Press, 2011.
3. Chris Bernhardt, Quantum Computing for Everyone, MIT Press, 2019.

Reference Books

1. David McMahon, Quantum Computing Explained, Wiley, 2008.
2. Kaye, Laflamme, Mosca, An Introduction to Quantum Computing, OUP, 2007. Scott Aaronson, Quantum Computing Since Democritus, CUP, 2013.
3. Susskind & Friedman, Quantum Mechanics: The Theoretical Minimum, Basic Books, 2014. Rosenblum & Kuttner, Quantum Enigma, OUP, 2011.
4. Benenti et al., Principles of Quantum Computation and Information, World Scientific, 2004. DST India and MeitY: Official Quantum Mission Reports, 2020 onwards.
5. Quantum Flagship EU: Roadmaps and Strategy Documents.

Online Learning Resources

1. IBM Quantum Experience & Qiskit Textbook Coursera – Quantum Mechanics and Quantum Computation (UC Berkeley) edX – Quantum Internet & Quantum Computers.
2. YouTube – Quantum Computing for the Determined (Michael Nielsen).

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(25EE2130) PEDAGOGY STUDIES

(Audit Course-II)

COURSE OBJECTIVES:

The objectives of this course

1. To enable the students to understand the aims, rationale, policy background, and conceptual frameworks in pedagogy, curriculum, and teacher education research.
2. To develop an understanding of diverse pedagogical practices
3. To make them learn the methodologies for assessing the effectiveness of pedagogical practices and teacher education models.
4. To enable them to learn professional development strategies, including peer support, community engagement, and alignment with curriculum and assessment.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Define and explain key concepts, frameworks, and methodologies in pedagogy and teacher education research.
2. Critically analyze pedagogical practices used in diverse classroom settings, with reference to teacher education and curriculum design.
3. Evaluate the effectiveness of pedagogical approaches using quality assessment tools and theory of change models.
4. Apply evidence-based strategies to improve classroom practices, curriculum alignment, and teacher professional development.
5. Identify and address barriers to learning through innovative pedagogical strategies.
6. Design and propose research studies that contribute to filling gaps in pedagogy, curriculum, and teacher education, with focus on dissemination and impact.

UNIT –I

Foundations of Pedagogy

Introduction to pedagogy and its importance in education - Historical and philosophical foundations of pedagogy - Theories of learning and teaching (behaviorist, cognitive, constructivist) - Role of pedagogy in shaping educational practices - Role of technology in modern pedagogy (ICT, e-learning, blended learning)

UNIT – II

Teaching-Learning Processes

Understanding the teaching-learning process - Lesson planning and curriculum design - Strategies for effective teaching and learning (expository, collaborative, experiential) - Use of technology to enhance teaching-learning processes (multimedia, simulations, gamification)

UNIT – III

Technology Integration in Education

Educational technology and system design - Instructional design models (ADDIE, ASSURE, Dick and Carey Model) - Emerging trends in e-learning (social learning, MOOCs, mobile learning) - ICT tools for teaching and learning (Learning Management Systems, online resources)

UNIT – IV

Pedagogy and Assessment

Pedagogy, pedagogical analysis, and assessment - Types of assessment (placement, formative, diagnostic, summative) - Technology-based assessment tools (online quizzes, polls, discussions) - Rubrics for self and peer evaluation- Reflective Practices

UNIT – V

Contemporary Issues and Trends

Inclusive education and technology (assistive technology, accessibility) - Change management and innovation in education - Quality assurance and evaluation in education (TQM, Six Sigma) - Future trends in pedagogy and technology (AI, AR, VR in education) - Personalized learning and adaptive teaching

Textbooks

1. Alexander, R. J. *Essays on Pedagogy*. Routledge, 2008.
2. Shulman, L. S. *The Wisdom of Practice: Essays on Teaching, Learning, and Learning to Teach*. Jossey-Bass, 2004

Reference Books

1. *Teaching for the Future: Effective Teacher Education and Pedagogical Practices*. OECD Publishing., 2021
2. Fullan, M., & Edwards, M. *System Change in Education: Sustainability and Impact*. Routledge, 2022.
3. Coe, R., Rauch, C., Kime, S., & Singleton, D. *Great Teaching Toolkit: Evidence Review*. Evidence Based Education., 2020
4. Zeichner, K. M. *The Struggle for the Soul of Teacher Education*. Routledge, 2024
5. UNESCO. *Global Education Monitoring Report: Pedagogy, Teachers and Learning*. UNESCO Publishing, 2024
6. Hattie, J. *Visible Learning: A Synthesis of Over 800 Meta-Analyses Relating to Achievement*. Routledge., 2009
7. Darling-Hammond, L. *Teacher Education Around the World: What Can We Learn from International Practice?* Routledge, 2007.

Online Resources

1. **UNESCO Education Resources** – https://www.unesco.org/education
2. **OECD Education and Skills** – https://www.oecd.org/education
3. **ERIC (Education Resources Information Center)** – https://eric.ed.gov (peer-reviewed papers, reports).
4. **World Bank Education** – https://www.worldbank.org/en/topic/education (research reports on teacher development in developing countries).
5. **NPTEL/SWAYAM MOOCs** – Teacher education and pedagogy-focused courses.
6. **Google Scholar Alerts** – set alerts for "pedagogical practices", "teacher education", "curriculum research" for the latest academic papers.

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(25EE2131) PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

(Audit Course-II)

COURSE OBJECTIVES:

The objectives of this course

1. To develop students' self-awareness by identifying their strengths, weaknesses, opportunities, and challenges (SWOC analysis).
2. To enable students to understand and apply the principles of emotional intelligence and effective interpersonal communication.
3. To cultivate positive thinking, resilience, mindfulness, and a growth-oriented mindset.
4. To enhance verbal and non-verbal communication skills, including confidence in public speaking and professional presentations.
5. To familiarize students with leadership styles, teamwork strategies, and collaborative problem-solving in personal and professional contexts.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Define and explain key concepts of self-awareness, personality, and personal growth.
2. Identify and apply strategies of emotional intelligence to regulate emotions and build effective interpersonal relationships
3. Demonstrate positive thinking, gratitude, and resilience to overcome personal and professional challenges
4. Analyze barriers to effective communication and apply verbal and non-verbal communication techniques in diverse contexts.
5. Prepare, deliver, and evaluate effective presentations and public speeches with confidence
6. Develop leadership and teamwork skills to collaborate, negotiate, and solve problems in group settings.

UNIT –I

Self-Awareness and Personal Growth

Understanding personality and its development- Identifying strengths, weaknesses, opportunities, and challenges (SWOC analysis)- Setting personal and professional goals- Practicing Self-Reflection and Journaling

(Activities: Personalitya assessments, self reflection exercises, group discussions, SWOC analysis worksheet, Action Plan, SMART goal activities, Reflective journaling, Self-care Planning)

UNIT – II

Emotional Intelligence and Interpersonal Skills

Understanding emotional intelligence and its importance - Developing self-awareness, self-regulation, and motivation - Building effective communication and interpersonal skills - Conflict resolution and negotiation strategies.

(Activities: Emotional Intelligence Quiz, Self-Reflection exercises, feedback sessions, mindfulness exercises, Positive self-talk, Active Listening exercises, conflict-resolution Role-play, Case studies & Group activities)

UNIT – III

Positive Thinking and Attitude

Understanding the power of positive thinking- Developing a growth mindset and resilience - Practicing gratitude and mindfulness- Overcoming negative thoughts and behaviors

(Activities on positive thinking, growth mindset, mindfulness and self-care plan for overcoming negative thoughts)

UNIT – IV

Effective Communication and Presentation Skills

Understanding the importance of effective communication- Developing verbal and non-verbal communication skills- Preparing and delivering effective presentations- Building confidence and public speaking skills

(Activities: Group discussions, Case studies, Role-Play, Non-verbal communication exercises, Practice presentations, Peer feedback, Public speaking exercises, Storytelling, Debates)

UNIT – V

Leadership and Teamwork

Understanding leadership styles and qualities - Developing leadership skills and qualities- Building effective teams and teamwork strategies- Practicing collaboration and problem-solving

(Activities: Case studies, Group discussions, Debates, Leadership role-playing, team building activities, Group projects, Collaborative problem-solving exercies, feedback sessions)

Textbooks

1. Daniel Goleman,*Emotional Intelligence: Why It Can Matter More Than IQ*, Bantam Books, 2017.
2. Stephen R. Covey, *The 7 Habits of Highly Effective People*, Simon & Schuster, 2020.

Reference Books

1. Dale Carnegie, *How to Win Friends and Influence People*, Simon & Schuster, 2020.
2. Brian Tracy, *Goals!: How to Get Everything You Want Faster Than You Ever Thought Possible*, Berrett-Koehler Publishers, 2021.
3. Robin Sharma, *The 5 AM Club: Own Your Morning, Elevate Your Life*, HarperCollins, 2020.
4. Carol S. Dweck, *Mindset: The New Psychology of Success*, Random House, 2016.
5. Daniel H. Pink,*Drive: The Surprising Truth About What Motivates Us*, Riverhead Books, 2018.
6. John C. Maxwell, *Leadershift: 11 Essential Changes Every Leader Must Embrace*, HarperCollins, 2019.

Online Resources

1. **Coursera** – *Personal Development Specialization* (https://www.coursera.org)
2. **edX** – *Leadership and Emotional Intelligence Courses* (https://www.edx.org)
3. **FutureLearn** – *Mindfulness and Resilience Training* (https://www.futurelearn.com)
4. **MindTools** – Practical resources on leadership, communication, and emotional intelligence (https://www.mindtools.com)
5. **Positive Psychology** – Articles and tools on resilience, gratitude, and well-being (https://positivepsychology.com)
6. **TED Talks** – Inspirational talks on leadership, communication, and self-growth (https://www.ted.com)
7. **Harvard Business Review (HBR)** – Leadership, negotiation, and workplace communication (https://hbr.org)

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(25CS5832) YOGA FOR STRESS MANAGEMENT

(Audit Course-II)

COURSE OBJECTIVES:

The objectives of this course

1. To make the students understand the foundational concepts of Yoga, including Ashtanga (eight limbs) as prescribed in classical texts.
2. To enable them analyze the principles of Yama and Niyama, and their role in ethical, personal, and social development.
3. To make them learn do's and don'ts of life through the practice of ahimsa, satya, astheya, brahmacharya, aparigraha, shaucha, santosh, tapa, swadhyaya, and ishwar-pranidhana.
4. To make them practice asanas and pranayama techniques for physical fitness, mental balance, and spiritual awareness.
5. To make them understand the holistic lifestyle through regular yoga practice, leading to personality development.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Explain the eight limbs of Yoga (Ashtanga) and their interrelationship in holistic development.
2. Demonstrate understanding of Yama and Niyama as ethical guidelines and apply them in personal and professional life.
3. Differentiate between do's and don'ts in daily life with reference to Yogic principles like ahimsa, satya, and swadhyaya.
4. Perform selected asanas and pranayama techniques with correct posture, breathing, and awareness.
5. Evaluate the physical, mental, and emotional benefits of yoga practices in stress reduction, concentration, and self-discipline.
6. Integrate yoga philosophy and practices into a personal routine for sustainable health and inner growth.

UNIT –I
Definitions of Eight parts of yoga.(Ashtanga)

UNIT – II
Yam and Niyam.

UNIT – III
Do's and Don'tsin life.

i. Ahinsa,satya,astheya,bramhacharya and aparigraha
ii. Shaucha,santosh,tapa,swadhyay,ishwarpranidhan

UNIT – IV
Asanand Pranayam

UNIT – V

i. Various yoga poses and their benefits for mind and body
ii. Regularization of breathing techniques and its effects-Types of pranayama

Textbooks

1. Swami Prabhavananda and Christopher Isherwood (translation & commentary), *Patanjali Yoga Sutras,*Sri Ramakrishna Math, 1953.
2. B.K.S. Iyengar, *Light on Yoga,* Thorsons, 2003.

Reference Books

1. T.K.V. Desikachar, *The Heart of Yoga: Developing a Personal Practice,* Inner Traditions 2nd Edition, 1999.
2. Acharya Yatendra, *Yoga & Stress Management*, Fingerprint Publishers, 2019
3. Yamini Muthanna, *The Power of Yoga,* Om Books International, 2015.
4. Nayaswami Devarshi, *Kriya Yoga: Spiritual Awakening for the New Age,* Ananda Sangha Publications, 2023.

Online Resources

1. **NPTEL / SWAYAM Online Courses** – Yoga and Physical Education modules.
2. **AYUSH Ministry Website**: https://yoga.ayush.gov.in – official yoga resources, protocols, and research.
3. **Yoga Journal**: https://www.yogajournal.com – practical guides, research updates, asana tutorials.
4. **Art of Living Foundation**: https://www.artofliving.org – pranayama, meditation, and wellness practices.
5. **YouTube Channels** (scholarly & practice-based):
   - *Sivananda Yoga Vedanta Centre*
   - *Yoga with Adriene* (for practical asana guidance)

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(25EC4223) Bi-CMOS TECHNOLOGY AND APPLICATIONS
(Program Elective-V)

COURSE OBJECTIVES:

The objectives of this course

1. To demonstrate in-depth knowledge in BiCMOS Technology.
2. To analyze complex engineering problems critically for conducting research in BiCMOS Technology.
3. To solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. To realize different digital circuits using BiCMOS Technology.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Demonstrate in-depth knowledge in BiCMOS Technology.
2. Analyze complex engineering problems critically for conducting research in BiCMOS Technology.
3. Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. Realize different digital circuits using BiCMOS Technology

UNIT – I

BiCMOS Process Technology: CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS and Bipolar Technologies, BiCMOS Technology, BiCMOS Design Rules.

UNIT – II

Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations.

BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT – III

Device Modeling: Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICE Models of the MOS Transistor, Analytical Model for Short-Channel MOS Devices.

Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-Moll Model, Bipolar Models in SPICE.

UNIT – IV

BiCMOS Digital Integrated Circuits: BiMOS Totem-Pole Inverter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates.

UNIT – V

BiCMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

Textbooks:

1. Sherif H.K. Embabi, Abdellati f Bellaouar & Mohamed I. Elmasry —Digital BiCMOS Integrated Circuit Design‖ Springer Science+Business Media, LLC.

2. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.

Reference Books:

1. Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2. James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press.
3. KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science.

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(25EC4224) OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN
(Program Elective-V)

COURSE OBJECTIVES:

The objectives of this course

1. To understand basics of statistical modeling.
2. To analyze performance of CMOS circuits with respect to power, area and speed.
3. To acquire complete knowledge regarding the various algorithms used for optimization of power and area.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand basics of statistical modeling.
2. Analyze performance of CMOS circuits with respect to power, area and speed.
3. Acquire complete knowledge regarding the various algorithms used for optimization of power and area.

UNIT – I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT – II

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT – III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floorplanning, wiresizing, Approximation and fitting-Monomial fitting, Max monomial fitting, Polynomial fitting.

UNIT – IV

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm Taxonomy- Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

UNIT – V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement – GA for ATG-problem encoding-fitness function-GA Vs

Conventional algorithm.

Textbooks:

1. Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

Reference Books:

1. Convex Optimization- Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004.

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(25EC4225) SoC ARCHITECTURE
(Program Elective-V)

COURSE OBJECTIVES:

The objectives of this course

1. To understand the basics related to SoC architecture and different approaches related to SoC Design.
2. To select an appropriate robust processor for SoC Design.
3. To select an appropriate memory for SoC Design.
4. To realize real time case studies.

COURSE OUTCOMES (COs):

On successful completion of this course, students will be able to

1. Understand the basics related to SoC architecture and different approaches related to SoC Design.
2. Select an appropriated robust processor for SoC Design
3. Select an appropriate memory for SoC Design.
4. Realize real time case studies.

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT – IV

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer.
2. Co-Verification of Hardware and Software for ARM System on Chip Design(Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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(25EC4226) IoT AND ITS APPLICATIONS
(Open Elective-I)

COURSE OBJECTIVES:
The objectives of this course
1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To implement the state of the Architecture of an IOT.
4. To compare IOT Applications in Industrial & real world.
5. To demonstrate knowledge and understand the security and ethical issues of an IOT.

COURSE OUTCOMES (COs):
On successful completion of this course, students will be able to
1. Apply the Knowledge in IOT Technologies and Data management.
2. Determine the values chains Perspective of M2M to IOT.
3. Implement the state of the Architecture of an IOT.
4. Compare IOT Applications in Industrial & real world.
5. Demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT – I
Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.
IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT – II
IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT – III
Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT – IV
Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT – V

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press,2015.

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence‖, Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.